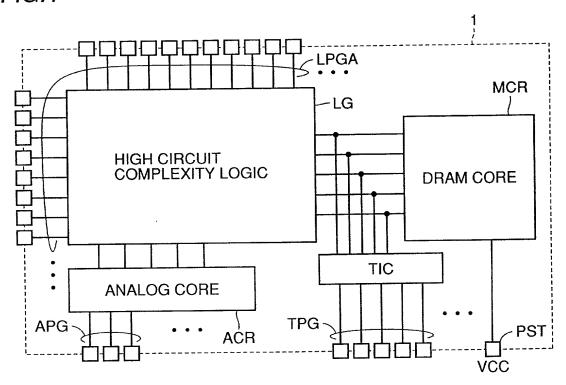
FIG.1



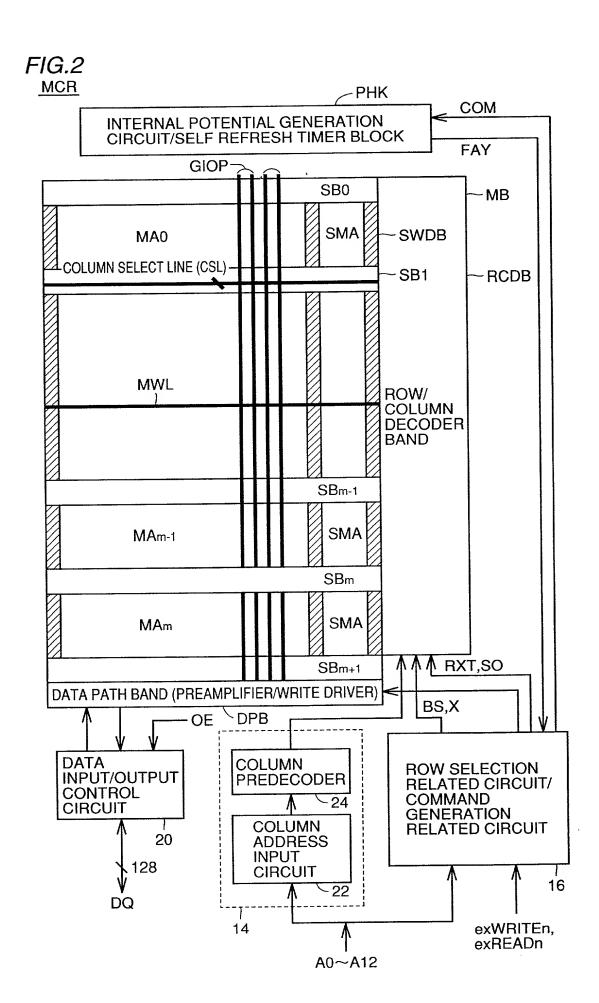


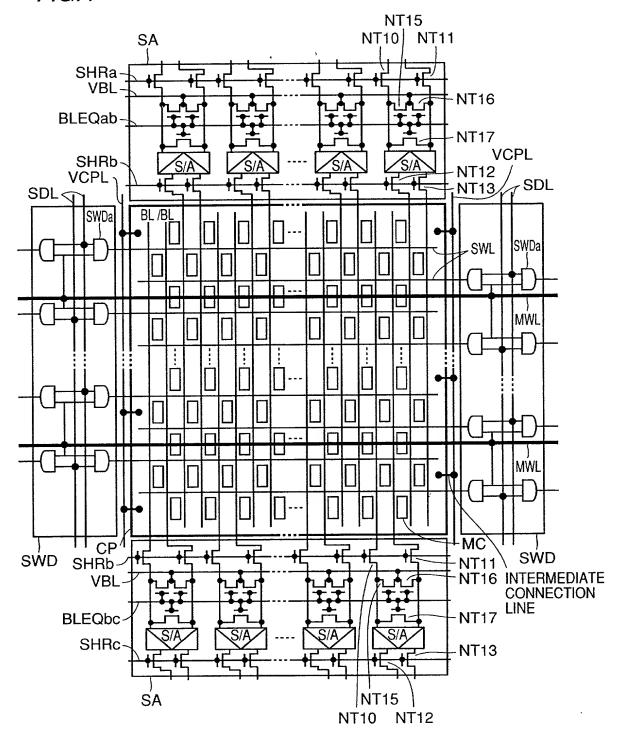
FIG.3

<u>MB</u>

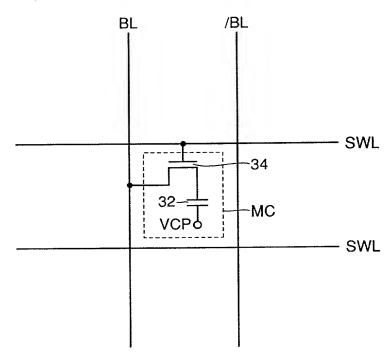
[SA		SA		SA			
SWD	SWL SWL MWL SMA	SWD	SWL SWL MWL	-0 -0 SWD	SWL	- O SWD	MWD	RD
L	SA		SA		SA			
SWD	SMA	SWD	SMA	SWD	SMA	SWD	MWD	RD
L	SA		SA		SA			
	SA	1	SA		SA			
SWD	SMA	SWD	SMA	SWD		SWD	MWD	RD
	SA		SA		SA			

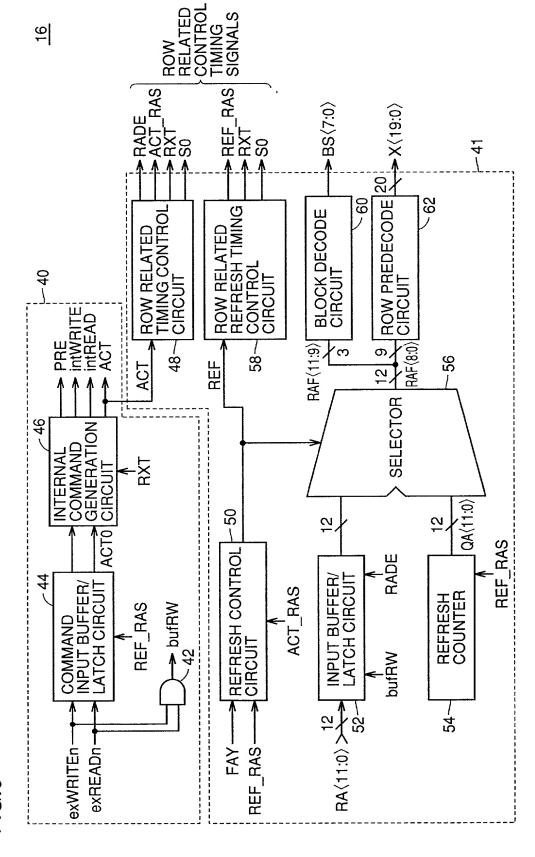
k X

FIG.4









F/G.6

FIG.7

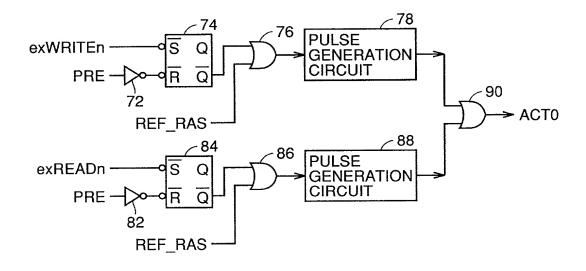
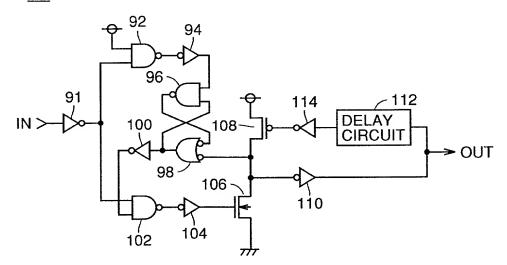


FIG.8

<u>78</u>



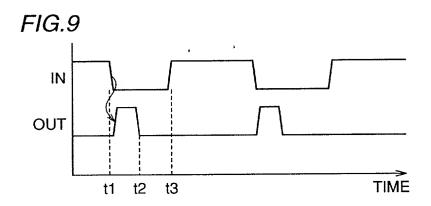


FIG.10

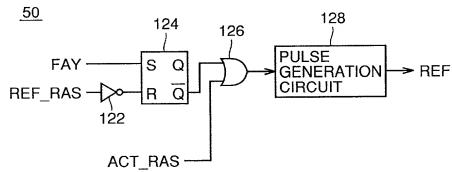


FIG.11

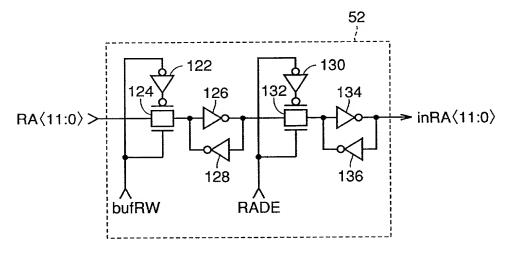


FIG.12

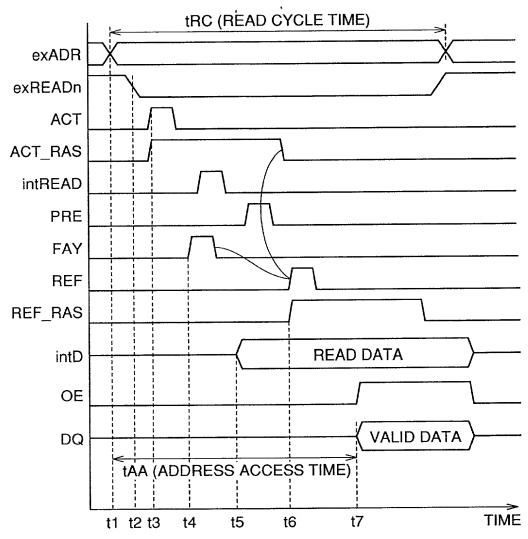


FIG.13

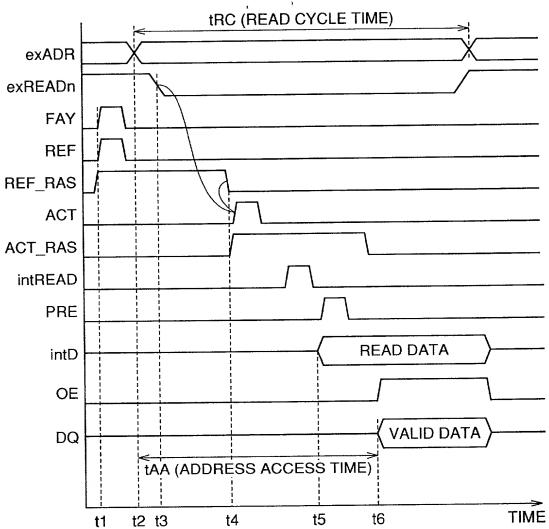


FIG.14

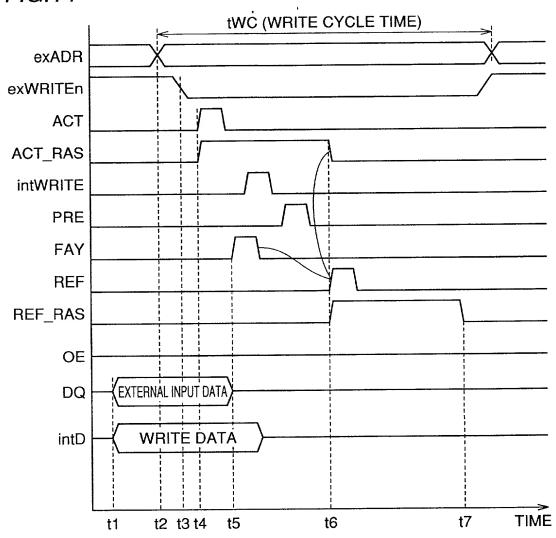
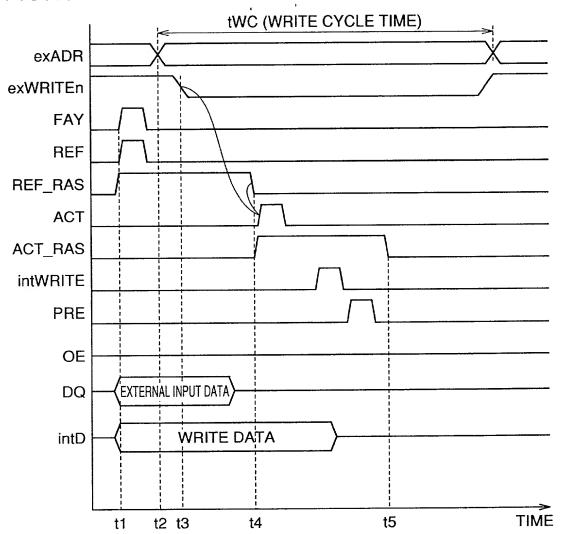


FIG.15





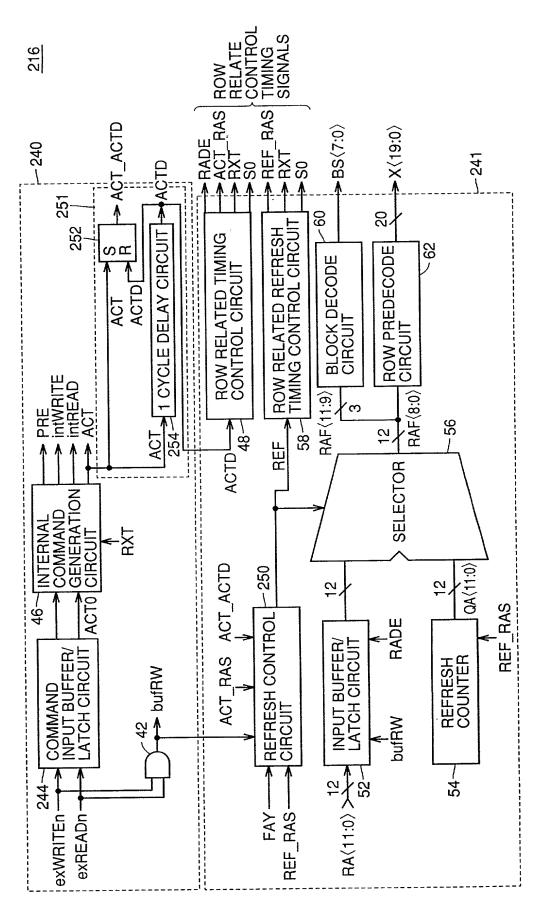


FIG.17

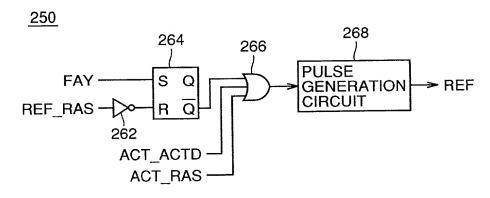


FIG.18

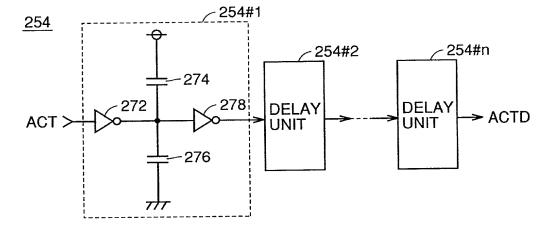
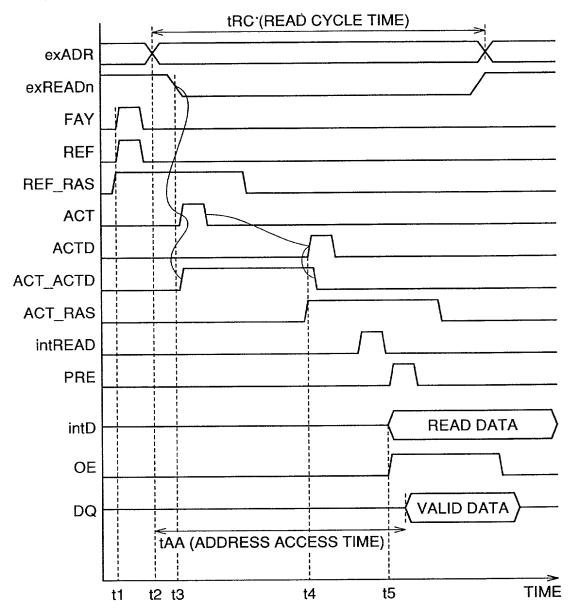


FIG.19





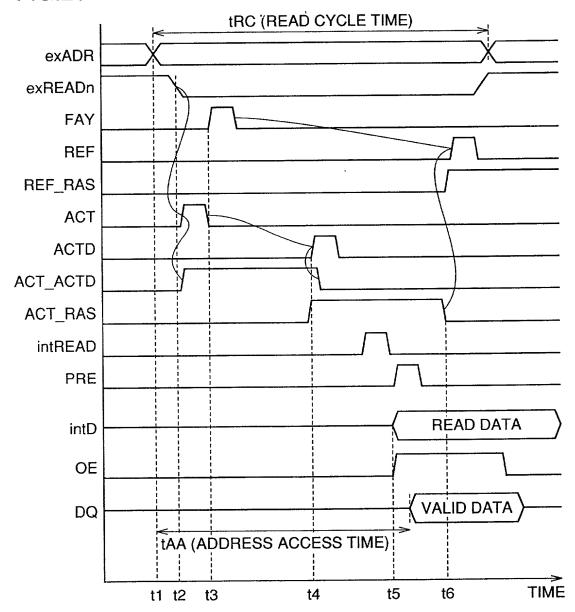


FIG.21 **MCRa** PHK COM INTERNAL POTENTIAL GENERATION CIRCUIT/SELF REFRESH TIMER BLOCK **FAY** GIOP SB0a - MBa MA0a SB1a -COLUMN SELECT LINE (CSL) -**RCDBa** RXT<1>, SO<1> SBm+1a SB0b - MBb **RCDBb** SB_{m-1}b **SMA** SBmb **SMA** RXT<0>. SO<0> SBm+1b DATA PATH BAND (PREAMPLIFIER/WRITE DRIVER) BS,X OE [►]DPB **DATA COLUMN ROW SELECTION** INPUT/OUTPUT PREDECODER RELATED CIRCUIT/ CONTROL **COMMAND** ~24 CIRCUIT **GENERATION** COLUMN RELATED CIRCUIT 20 **ADDRESS INPUT** 128 **CIRCUIT** 316 -22 DQ 14 exWRITEn, exREADn A0~A12

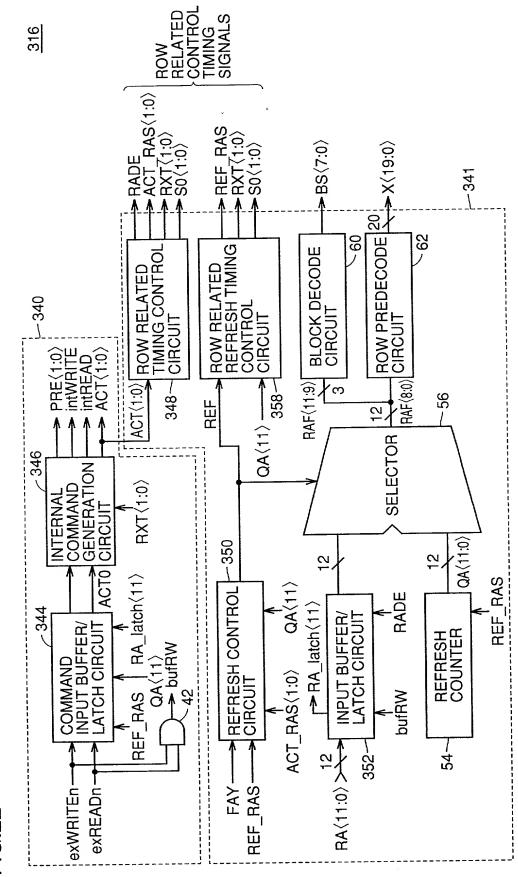
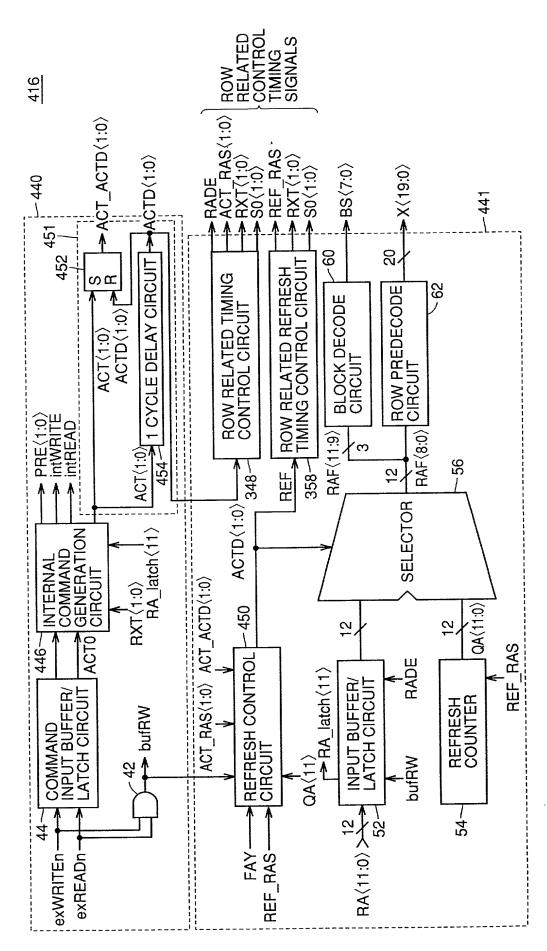


FIG.22





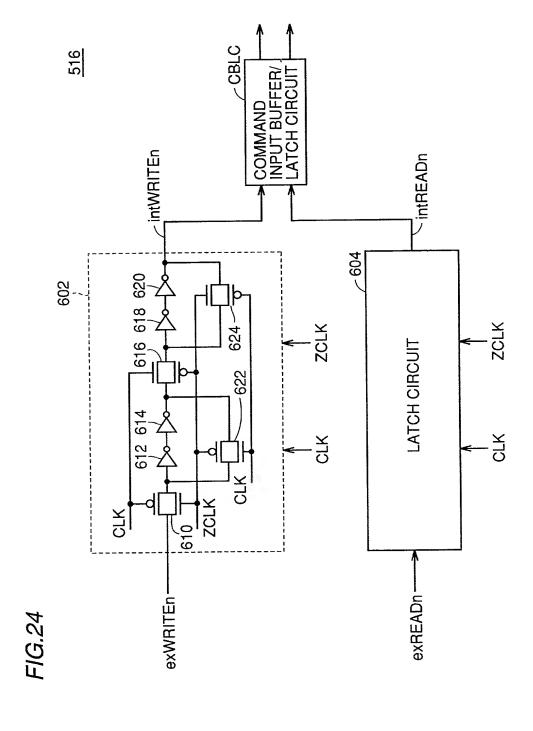
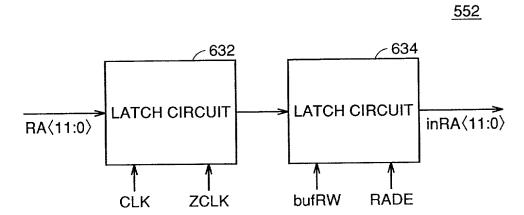


FIG.25



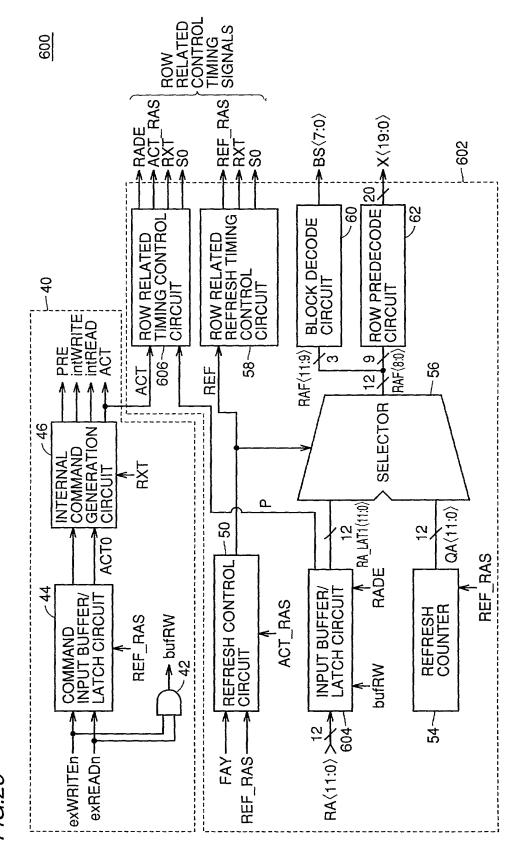
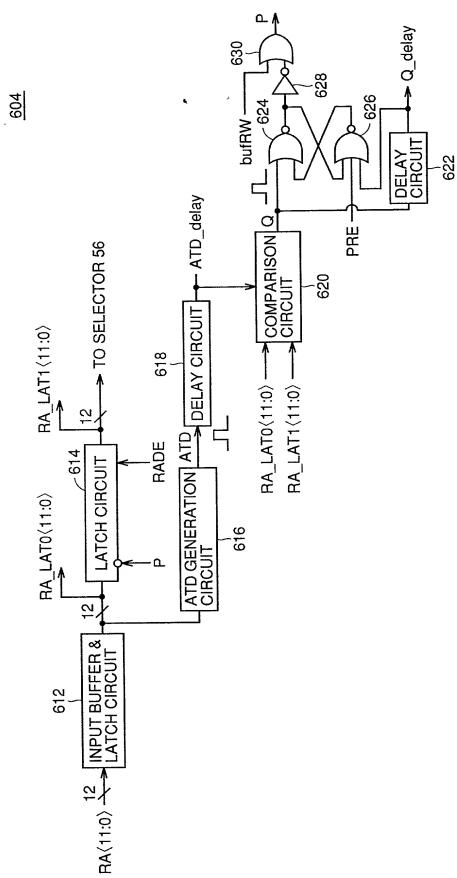


FIG.26





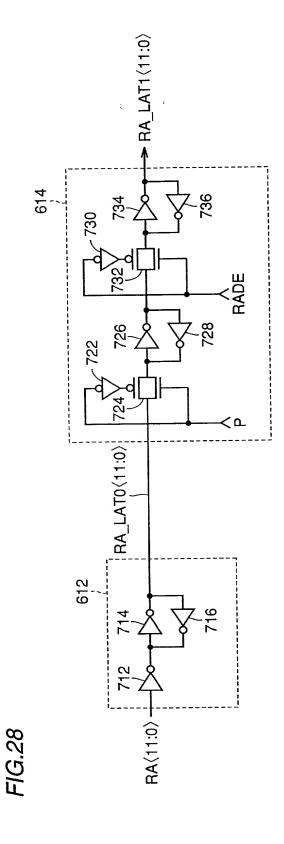


FIG.29

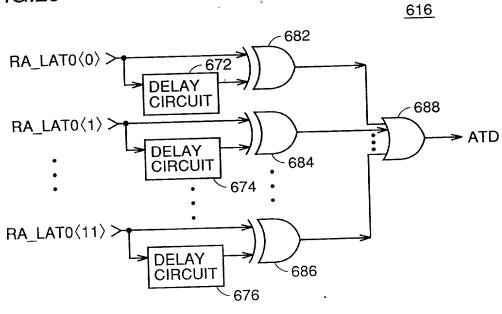


FIG.30

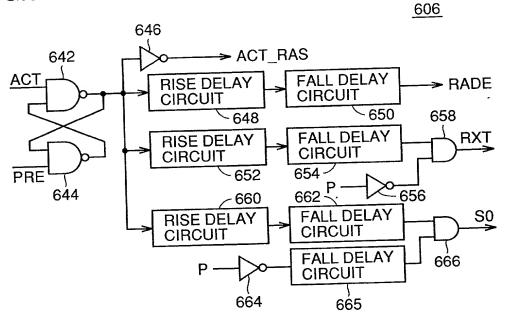
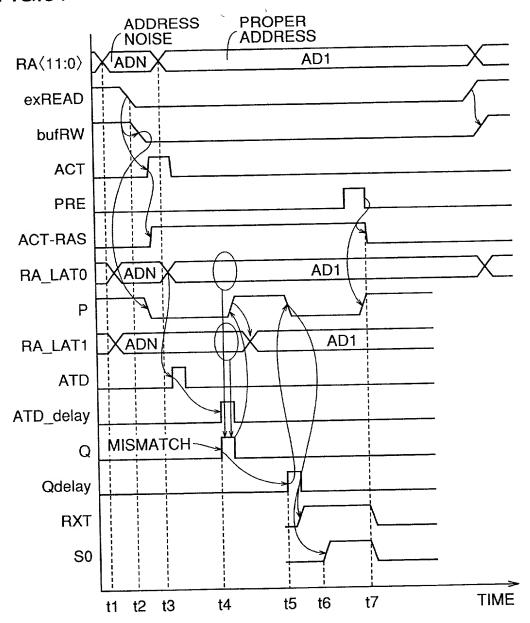
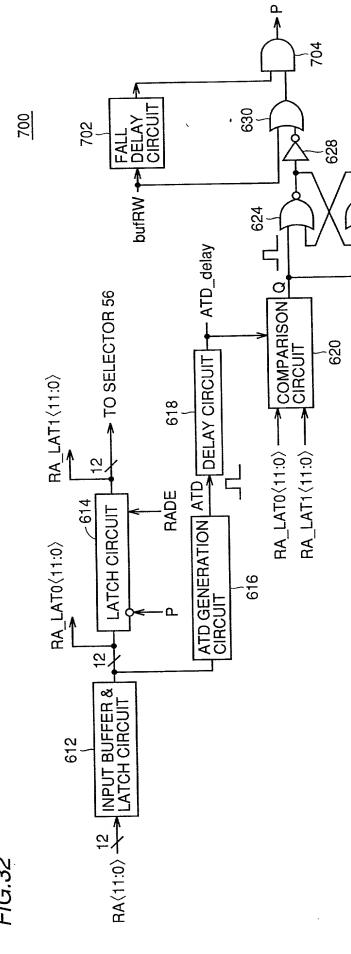


FIG.31





-626

PRE-

DELAY CIRCUIT

622

(



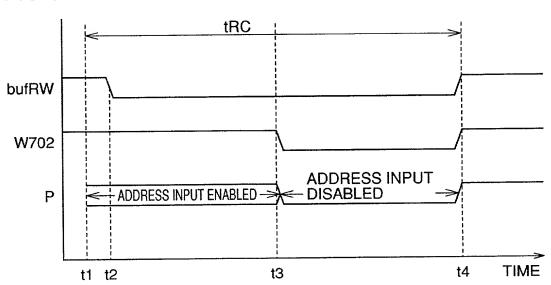


FIG.34 PRIOR ART

